

AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A method, comprising:

providing power to an integrated circuit (IC) during an active mode;

moving an integrated circuit state of the IC into on-die storage of the IC;

and

externally disabling power to on-die combinational circuitry during a low power mode by disrupting power supplied from an external power supply regulator to the IC.

2. (Original) The method of claim 1, wherein disabling power further includes tri-stating an output of a power supply regulator that provides power to the on-die combinational circuitry.

3. (Original) The method of claim 1, wherein disabling power further includes gating an off-die clamp to disrupt power supplied from an external power supply regulator to the on-die combinational circuitry.

4. (Currently Amended) The method of claim 1, wherein disabling disrupting ~~the~~ power further includes gating an on-die clamp ~~to disrupt power supplied from an external power supply regulator to the on-die combinational circuitry.~~

5. (Original) The method of claim 1, further including reapplying power after the integrated circuit receives an interrupt.

6. (Original) The method of claim 1, further including:
supplying the power from a power supply regulator along a path to the on-die combinational circuitry; and
providing a feedback signal from the path to the power supply regulator.

7. (Currently Amended) A method comprising:
forcing a high impedance state on an output of a power supply regulator that is coupled to a power pin of an integrated circuit,
wherein forcing the high impedance state includes de-asserting a drive pin coupled to a gate of a MOS power transistor to force the high impedance state on the output of the power supply regulator.

8. (Cancelled)

9. (Currently Amended) The method of claim 8 7 further comprising:
connecting a diode to a source of the MOS power transistor.

10. (Original) The method of claim 7 further comprising:
timing the de-assertion to avoid high voltages on a supply inductor
coupled between the output of the power supply regulator and the power pin of the
integrated circuit.

11. (Currently Amended) A circuit comprising:
a first terminal of an integrated circuit (IC) coupled to receive power for on-die
combinational circuitry when the integrated circuit is in an active mode and to not
receive power when the integrated circuit is in a low power mode; and
a second terminal to receive power supplied to circuitry for low power logical
state retention of the IC when the integrated circuit is in the low power mode, wherein
the second terminal provides power to low-leakage memory that stores the logical state.

12. (Original) The circuit of claim 11 further comprising:
a transistor external to the integrated circuit to gate the power received at the
first terminal.

13. (Original) The circuit of claim 12, wherein the transistor is coupled to a
power regulator and switched off when the integrated circuit is in the low power mode.

14. (Original) The circuit of claim 11 wherein a feedback signal is taken from
the first terminal and supplied to a power regulator.

15. (Original) The circuit of claim 11 wherein a feedback signal is taken from within the integrated circuit and supplied to a power regulator.

16. (Original) The circuit of claim 11 further including a multiplexer to receive a signal taken from within the integrated circuit and a signal external to the integrated circuit, where an output of the multiplexer is coupled to a power regulator.

17. (Original) The circuit of claim 11 further comprising:
a transistor internal to the integrated circuit to gate the power received at the first terminal and float an internal power conductor connected to combinational logic.

18. (Currently Amended) A system comprising:
an integrated circuit having a power terminal coupled through an external control transistor to an output of a power supply; and
a multiplexer that selectively connects an external power signal supplied at a pin of the integrated circuit, an internal power signal of the integrated circuit, and a power signal supplied to the external control transistor to the power supply.

19. (Original) The system of claim 18 wherein the control transistor is an NMOS transistor.

20. (Original) The system of claim 18 wherein the control transistor is a CMOS pass gate.

21. (Cancelled)

22. (Currently Amended) The system of claim 21 18 wherein the multiplexer disconnects the power signal from the power supply while the integrated circuit is in a low power standby mode.